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EXAMINER

LE, LANA N

ART UNIT

PAPER NUMBER

2618

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/791,551

Applicant(s)

HARA, YOSHITAKA

Examiner

Lana N. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,7 and 12-19 is/are rejected.
- 7) ☒ Claim(s) 3-6 and 8-11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

0DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Jagger et al (US 6,807,405).

Regarding claim 1, Jagger et al disclose a high frequency device (figs. 6, 5), comprising:

a first filter (2nd filter block from figure 5 shown in figure 6 of first filter module 61) for extracting signal components in a predetermined frequency band from an input signal;

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a frequency converter (3rd mixer in second filter module 61) for converting a frequency of the signal components extracted by the first filter;

a second filter (3rd filter block of second filter module 61 shown in fig. 6) for extracting signal components in a predetermined frequency band from the signal components with a frequency thereof converted by the frequency converter;

a bypass circuit (when switch closed inside second block 61, signal connection line from 3rd mixer to 4th filter) for detouring the second filter downstream of the first filter;

a switching mechanism (switch inside block 61) including a switching circuit for switching connection of a signal path downstream of the first filter to either the second filter (when switch is open) or the bypass circuit (connection line from 3rd mixer to 4th filter).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2, 7, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagger et al (US 6,807,405) in view of Hasegawa (JP 03,179,825).

Regarding claim 2, Jagger et al disclose the high frequency device according to claim 1, wherein Jagger et al do not disclose the switching mechanism includes,

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downstream of the second filter, a switching circuit for switching the signal path.

Hasegawa discloses a switching mechanism (5, 6) includes, downstream of the second filter (IF filter 2b wherein the RF front end circuit 2a may contain a first RF filter as is well known in the art), a switching circuit (6) for switching the signal path (constitution; fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a switching circuit downstream of the second filter in order to either connect the output of the bypass circuit or the filter output to the downstream signal path to adjust the receiver to an optimum point as suggested by Hasegawa.

Regarding claim 7, Jagger et al disclose the high frequency device according to claim 1, wherein Jagger et al do not disclose the switching mechanism includes, switching circuits provided upstream and downstream of the second filter, respectively, for switching the signal path. Hasegawa discloses switching circuits (5 and 6) provided upstream (5) and downstream (6) of the second filter (IF filter 2b wherein the RF front end circuit 2a may contain a first RF filter as is well known in the art) respectively, for switching the signal path (constitution; fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a switching circuit upstream and downstream of the second filter in order to either connect the input and output of the bypass circuit or the filter's input and output to the downstream signal path to adjust the receiver to an optimum point as suggested by Hasegawa.

Regarding claim 12, Jagger et al and Hasegawa disclose the high frequency device according to claim 7, wherein the frequency converter (3rd filter block of second filter module 61 shown in fig. 6) is provided upstream of the switching circuit (switch

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inside second filter module 61 shown in fig. 6), wherein Hasegawa discloses the switching circuit (6) is provided upstream of the second filter. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a switching circuit upstream of the second filter in order to either connect the input of the bypass circuit or the filter to the downstream signal path to bypass the filter to the detector circuit when no interfering signal needs to be filtered.

Regarding claim 14, Jagger et al and Hasegawa disclose the high frequency device according to claim 12, wherein Hasegawa discloses the bypass circuit () is biased via a resistor (7c) so as to have a source power potential (+B).

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jagger et al (US 6,807,405) in view of Hasegawa (JP 03,179,825) and further in view of Mizusawa et al (US 6,038,428).

Regarding claim 13, Jagger et al and Hasegawa disclose the high frequency device according to claim 12, wherein Jagger et al and Hasegawa do not disclose the frequency converter variably controls a frequency changing amount according to a frequency of a signal input to the frequency converter so that signals having a constant frequency are output. Mizusawa et al disclose a frequency converter variably controls a frequency changing amount according to a frequency of a signal input to the frequency converter so that signals having a constant frequency are output (col 5, line 61 – col 6, line 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a constant output in order to control the output of the

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frequency converter to stability to reduce the need of using the filter of Yamamoto to reduce power consumption.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jagger et al (US 6,807,405) in view of Hasegawa (JP 03,179,825) in view of Yamamoto et al (2002/0,089,608) and further in view of Miyazaki (US 5,802,447).

Regarding claim 15, Jagger et al and Hasegawa disclose the high frequency device according to claim 12, wherein Jagger et al and Hasegawa do not disclose the second filter is formed as a unit separate from an integrated circuit which includes the frequency converter and the switching circuit an integrated circuit. Yamamoto et al disclose an IC (second IC shown by 2nd block via dotted lines) which includes a frequency converter (14) and a switching circuit (17) for switching a filter (16) (col 5, line 66 – col 6, line 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have receiving components integrated into an IC in order to have circuit miniaturization for device compactability. Jagger et al, Hasegawa, and Yamamoto et al do not disclose the second filter is formed as a unit separate from an integrated circuit. Miyazaki discloses a second filter (37) is formed as a unit separate from an integrated circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the filter as a separate unit from the IC in order to more accurately pass the signals in a required band.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al (US 2002/0,089,608) in view of Hidefumi (JP 05-304485) and further in view of Mizusawa et al (US 6,038,428).

Regarding claim 16, Yamamoto et al disclose a tuner high frequency device (10 receiving high frequency via amplifier 12; figs. 2 & 4), comprising:

a frequency converter (14) for converting a frequency of the signal components extracted by the first amplifier 12 to thereby obtain an IF signal (IF), a filter (16) for extracting signal components in a predetermined frequency band from the IF signal obtained by the frequency converter (14);

a bypass circuit (filter (filter bypass connection from 17a via signal line to SAW filter 20, fig. 4) for detouring the filter downstream of the first amplifier 12; a switching mechanism (17) including a switching circuit (17) for switching connection of a signal path downstream of the first amplifier to either the second filter or the bypass circuit.

Yamamoto et al do not disclose a first radio frequency filter for extracting signal components in a predetermined frequency band from an input signal having a radio frequency. Hidefumi discloses an RF filter (51) upstream of the frequency mixer (54) and the second filter (11; figs. 1&2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an RF filter in order to filter the high unwanted radio frequency signals to reduce interference coming into the mixer.

Yamamoto et al and Hidefumi do not disclose the frequency converter variably controls a frequency changing amount according to a frequency of a signal input to the frequency converter so that signals having a constant frequency are output. Mizusawa et al disclose a frequency converter variably controls a frequency changing amount according to a frequency of a signal input to the frequency converter so that signals having a constant frequency are output (col 5, line 61 – col 6, line 2). It would have

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been obvious to one of ordinary skill in the art at the time the invention was made to have a constant output in order to control the output of the frequency converter to stability to reduce the need of using the filter of Yamamoto and Hidefumi to reduce power consumption.

8. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidekuni et al (JP 2001-024619) in view of Yamamoto et al (US 2002/0,089,608).

Regarding claim 17, Hidekuni et al disclose a signal receiver (figs. 21-22) comprising:

a frequency converter (9, 9'; fig. 21) for converting frequency of signal components extracted using a first filter (LPF 7 of figure 22; wherein the A/D converter 8 and henceforth of figure 22 is replaced with the circuit of figure 21) which extracts signal components in a predetermined frequency band from an input signal;

a bypass circuit (connection line from 45 to input of 43) for detouring a second filter (42, 42') which extracts signal components from a front end circuit (2a) in a predetermined frequency band from the signal components with a frequency thereof converted by the frequency converter (9, 9'); and

a switching mechanism (45, 45') including a switching circuit for switching connection of a signal path downstream of the first filter (7) to either the second filter (42, 42') or the bypass circuit (connection line from 45 to input of 43).

Hidekuni et al do not disclose an integrated circuit comprising the frequency converter, bypass circuit and switching mechanism. Yamamoto et al discloses an integrated circuit (tuner IC 10; fig. 2) comprising the frequency converter (14), bypass circuit (filter

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bypass connection from 17a via signal line to SAW filter 20, fig. 4) and switching mechanism (17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the receiving components integrated into an IC in order to have circuit miniaturization for device compactability.

Regarding claim 19, Hidekuni et al and Yamamoto et al disclose the integrated circuit according to claim 17, wherein Yamamoto et al disclose the IC comprising an external connection terminal (terminal at switching circuit 17) via which to input a control circuit (60) for controlling the switching by the switching circuit (17) (fig. 2).

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hidekuni et al (JP 2001-024619) in view of Yamamoto et al (US 2002/0,089,608) in view of Miyazaki (US 5,802,447) and further in view of Yamamoto et al (US 6,308,047).

Regarding claim 18, Hidekuni et al and Yamamoto et al disclose the integrated circuit according to claim 17, wherein Hidekuni et al and Yamamoto et al do not disclose the second filter being formed as a unit separate from the integrated circuit. Miyazaki disclose an IC (second IC shown by 2nd block via dotted lines) wherein a second filter (37) being formed as a unit separate from the integrated circuit (second IC) (col 5, line 66 – col 6, line 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the filter as a separate unit from the IC in order to more accurately pass the signals in a required band. Hidekuni et al, Yamamoto et al and Miyazaki do not explicitly disclose the IC comprising a terminal for connecting the second filter. Yamamoto et al (US 6,308,047) disclose the IC comprising a terminal for connecting a filter outside front end IC (col 3, lines 51-63). It would have been obvious

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to one of ordinary skill in the art at the time the invention was made for Miyazaki to have a connection terminal in order to connect the filter outside the IC to the IC.

Allowable Subject Matter

10. Claims 3-6 and 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 3, Jagger et al disclose the high frequency device according to claim 2, wherein Jagger et al and the cited prior art fail to disclose the frequency converter includes a first frequency converter provided upstream of the second filter and a second frequency converter provided to the bypass circuit.

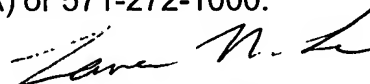
Regarding claim 8, Jagger et al and Hasegawa disclose the high frequency device according to claim 7, wherein Jagger et al, Hasegawa and the cited prior art fail to disclose the frequency converter includes a first frequency converter provided upstream of the second filter and a second frequency converter provided to the bypass circuit.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 9:30-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


6-07-06

Lana Le

LANA LE
PRIMARY EXAMINER